HEART 2018 Program

Day 1 (June 20th, Wed)		
8:00-8:50	Breakfast	
8:50-9:00	Opening	Chairs: Jason Anderson and Yuko Hara
9:00-9:45	Invited Talks	Chair: Yuko Hara
	Prof. Keith Vanderlinde (Dunlap Institute)	Digitally Mapping the Universe
9:45-10:30	Dr. Andrew Ling (Intel Corp.)	Why FPGAs Are the Perfect Spatial Processor for Deep Learning Acceleration
10:30-11:00	Coffee Break	
11:00-12:15	Session 1: HW-SW Partitioning and Optimization Frameworks	Chair: Martin Herbordt
	Wibheda: Framework for Data Dependency-aware Multi-constrained Hardware-Software Partitioning in FPGA-based SoCs for IoT Devices	Deshya Wijesundera, Alok Prakash, Thilina Perera, Kalindu Herath and Thambipillai Srikanthan
	A Recurrently Generated Overlay Architecture for Rapid FPGA Application Development	David Wilson, Greg Stitt and James Coole
	High-productivity Programming and Optimization Framework for Stream Processing on FPGA	Jinpil Lee, Tomohiro Ueno, Mitsuhisa Sato and Kentaro Sano
12:15-13:45	Lunch	
13:45-14:30	Invited Talk	Chair: Tomasz Czajkowski
	Dr. Martin Snelgrove (Untether AI)	Near-Memory and In-Memory Inference
14:30-15:00	Poster talks (5 min X 6 talks)	Chair: Andy Ye
15:00-16:15	Poster Session and Coffee Break	
	A Case Study of Integer Sum Reduction using Atomics	Zheming Jin and Hal Finkel
	An FPGA-Based Hardware Accelerator for K-Nearest Neighbor Classification for Machine Learning on Mobile Devices	Mokhles A. Mohsin and Darshika G. Perera
	Scalable Open-Source Reconfigurable Architecture for Bacterial Quorum Sensing Simulations	Alan Ehret, Peter Jamieson and Michel A. Kinsy
	FPGA Hardware Implementation and Optimization for Neural Network based Chaotic System Design	Lei Zhang and Jesse Schmitz
	Flexible Reconfigurable On-chip Networks for Multi-core SoCs	Masoud Oveis-Gharan and Gul Khan
	A Performance Per Power Efficient Object Detector on an FPGA for Robot Operating System	Haoxuan Cheng, Shimpei Sato and Hiroki Nakahara

16:15-17:05	Session 2: Acceleration	Chair: Hiroki Nakahara
	Accelerating Space Radiate Transfer on FPGA using OpenCL	Norihisa Fujita, Ryohei Kobayashi, Yoshiki Yamaguchi, Yuuma Oobata, Taisuke Boku, Makito Abe, Kohji Yoshikawa and Masayuki Umemura
	FPGA HPC using OpenCL: Case Study in 3D FFT	Ahmed Sanaullah and Martin Herbordt
18:15/18:30	Departure for banquet boat tour from conference venue	Walking departure: 18:15; transit departure: 18:30 (student volunteers will lead the way)
19:00-22:00	Banquet on boat (incl. Best Paper Awards announced on boat)	Boat boarding: 7pm; departure: 7:30pm

Day 2 (June 21st, Thu)		
8:45-9:25	Breakfast	
9:25-9:30	Opening	
9:30-10:15	Invited Talk	Chair: Nachiket Kapre
	Dr. Jongsok James Choi (LegUp Computing Inc.)	Accelerating Memcached with Cloud-Deployed FPGAs
10:15-10:45	Coffee Break	
10:45-12:25	Session 3: Applications	Chair: Lei Zhang
	Swap-Based Merge Network for High Performance Sorting Accelerators	Kenji Kise
	CJS: Custom Jacobi Solver	Andreea Ingrid Cross, Liucheng Guo, Wayne Luk and Mark Salmon
	Power Efficient Object Detector with an Event-Driven Camera on an FPGA	Masayuki Shimoda, Shimpei Sato and Hiroki Nakahara
	HLS-based FPGA Acceleration of Light Propagation Simulation in Turbid Media	Abdul-Amir Yassine, Yasmin Afsharnejad, Omar Ragheb, Vaughn Betz and Paul Chow
12:25-14:00	Lunch	
14:00-14:45	Invited Talk	Chair: Jason Anderson
	Niles Burbank (AMD)	GPUs as the Catalyst for Innovation in Artificial Intelligence
14:45-15:15	Coffee Break	
15:15-16:30	Session 4: Architectures and Overlays	Chair: Kentaro Sano
	Use of CPU Performance Counters for Accelerator Selection in HLS-Generated CPU-Accelerator Systems	Bain Syrowik, Blair Fort and Stephen Brown
	Real Chip Evaluation of a Low Power CGRA with Optimized Application Mapping	Takuya Kojima, Naoki Ando, Yusuke Matsushita, Hayate Okuhara, Nguyen Anh Vu Doan and Hideharu Amano
	Low-Latency FIR Filter Structures Targeting FPGA Platforms	Marcel Eckert, Bernd Klauer, Udo Zölzer, Piero Rivera Benois and Patrick Nowak

Day 3 (June 22nd, Fri)		
8:15-9:00	Breakfast	
9:00-13:00	Xilinx hands-on workshop	Instructor: Parimal Patel
	FPGA-based Accelerated Cloud Computing with AWS EC2 F1 and SDAccel	